# IMPACT OF HIGH K MATERIALS & DESIGN OF STRUCTURES FOR SUPPRESSING LEAKAGE MECHANISM IN NANO SCALE FET ARCHITECTURES

**A SYNOPSIS**

*Submitted by*


**K. KALAI SELVI**

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**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

**SCHOOL OF ELECTRONICS AND ELECTRICAL TECHNOLOGY**

**KALASALINGAM ACADEMY OF RESEARCH AND EDUCATION**

(DEEMED TO BE UNIVERSITY)

**ANAND NAGAR, KRISHNANKOIL – 626 126**

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## 1. INTRODUCTION

Due to traditional scaling, the semiconductor sector for the past 50 years, is in fact starting to exhibit the basic limitations of the materials that make up the planar complementary metal oxide semiconductor (CMOS) process building blocks. Geometrical Scaling (1975-2002) refer to reduction of vertical and horizontal dimensions of planar transistors with improved performance. To further extend the device scaling strategy, new materials can be added to the basic CMOS structure to replace and/or supplement the existing ones. This regime has frequently been referred to as "Equivalent Scaling" (2003-2024) since the incorporation of these new materials into the modified CMOS process improves electrical performance for device physicists and circuit designers similar to historical patterns. 3D power scaling (2025-2040) transition to fully developed vertical device structures. Technology advancements are driven by heterogeneous integration and lower power usage. Low k dielectric oxide preferably $SiO_2$ was used since the MOSFET was invented in 1960 because of its thermal stability and electrical stability at the junction between $SiO_2$ and silicon (Si). The silicon has low dielectric constant of 3.9. To create tiny and high-speed integrated circuits, the $SiO_2$ gate dielectric's physical thickness and gate length are reduced. As gate dielectric thickness falls below 1.2 nm the leakage current in gate will increase due to direct tunneling of electrons and the power dissipated in the circuit will increase to unbearable levels. A high - K gate dielectric could be used as a potential solution. In order to preserve the downward scaling of threshold voltage ($V_{TH}$), materials with k>3.9 are investigated for the dielectric in FET devices, which significantly alters threshold voltage. Some of them are Hafnium dioxide ($HfO_2$) (25), Zirconium dioxide ($ZrO_2$) (25), and Aluminium oxide ($Al_2O_3$) (9), Silicon nitrate ($Si_3N_4$) (7). These materials have high dielectric constants (high k), as their name would imply, which enhance oxide capacitance. They also have low gate leakage currents, which increase device stability and result in lower power dissipation and higher breakdown voltage. Leakage current increases as MOSFET parameters such as oxide thickness, channel width and channel length continuously shorten and ended in a number of short channel defects- including hot carriers, drain induced barrier lowering (DIBL), degradation in mobility of charges and other phenomena. Alternatively easily fabricated transistors such as junctionless and tunnel FETs have been evaluated to overcome these issues and enable the MOSFET to obtain subthreshold swing lower than 60 mV/dec at normal temperature.

## 2. LITERATURE REVIEW

Ratul Kumar Baruah and Roy Paily [1] in 2015 reported that in Junctionless Field effect transistor (JLFET) high k material like $HfO_2$ can be used as a dielectric substance in place of $SiO_2$ due to its excellent property of reduced oxide thickness having reduced gate tunneling leakage, and immune to short channel effect.

Junctions disappear when the concentration and doping in all the regions of FET are identical, as demonstrated by Chi-Woo Lee et al. [2] in 2010. In comparison to inversion-mode devices, the Junctionless MuGFETs (Multigate FET) seems to be less sensitive to changes in specific process parameters. The current drive of Junctionless MuGFETs was improved by using additional source and drain doping. It seems that regulating the cross section is an important aspect for threshold voltage modification.

Colinge et al. [3] in 2011 explained transistors without junctions or doping concentration gradients are also known as gated resistors or junctionless transistors. These devices are created with silicon nanowires and have complete CMOS functionality. A Junctionless transistor is essentially an on-state device in which the thermodynamic energy separation between the metal gate and the semiconductor changes the flat band voltage and the turn on voltage to non- negative values. When switched on and operating at flat band, the device functions essentially like a resistor, with the E- field normal to the charge movement in the device being nearly equal to zero.

Arian Nowbahari et al. [4] in 2020 concluded that junctionless transistors are capable of supporting reduced drain induced barrier lowering (DIBL), less subthreshold swing, large $I_{ON}/I_{OFF}$ value.

Suresh Gundapaneni et al. [5] in 2011 demonstrated the implantation of high dielectric constant material in JLFET gate enhanced the fringing electric fields by causing depletion in the off state beyond the gate edges. As a result the extended channel offered superior sub threshold properties. Enhanced depletion at the source-channel junction resulted in increased barrier height whereas in a typical MOSFET, this is because of the pn junction. Additionally, the physical gate length was less than the effective gate length. Therefore, less leakage current was achieved by the device with the high k spacer.

Suresh Gundapaneni et al. [6] in 2011 concluded that JLFETs can ease the stacking of metal gate because they don't require incredibly precise source/drain implants and anneals. In order for them to function optimally, they require costly, thin device layers that are difficult to produce technologically.

Konrad Young [7] in 1989 illustrated that threshold voltage in SOI MOSFETs can be reduced by reducing the thickness of the silicon film. MOSFETs have an advantage over their bulk-silicon counterparts in terms of the threshold voltage drop brought on by short channels.

Anurag Chaudhry and Jagadesh Kumar [8] in 2004 revealed that increasing drain voltage reduces the barrier height for carriers. Consequently, the off-current rises as more carriers transport from the source towards the channel. The output current is influenced by voltages at gate and drain. Short channel effect (SCE) is mostly caused by the DIBL effect, which reduces the on voltage as the length of device decreases. Substrate biasing, buried oxide thickness thin-film doping density and thin-film thickness all affect SCE in an SOI device. Fully depleted Silicon on insulator MOSFETs employ thinner silicon sheets to block subsurface leakage channels, therefore lowering SCEs. Employing dual-material gates in FETs reduced the carrier velocity in the device and diminished the SCE.

Suresh Gundapaneni et al. [9] in 2012 demonstrated that the length of the channel, thickness of the silicon body and the doping of JLT all strongly influence tunneling current.

Partha Mondal et al. [10] in 2013 said by reducing doping vertically, conductivity at the lower portion of the device can be reduced, preventing unwanted current from passing through bottom of the device. An SOI-based junctionless transistor with nonuniform channel concentration improved the leakage current and consequently, the $I_{ON}/I_{OFF}$ ratio.

Ratul Kumar Baruah and Roy Paily [11] in 2013 indicated that because of the junction-free design and lack of doping concentration gradient, the junctionless field effect transistor is a potential device in VLSI.

Shubham Sahay and Mamidala Jagadesh Kumar [12] in 2017 found the introduction of parasitic bipolar effect when charge transportation between bands occurred at the channel-drain interface of silicon-on-insulator JLFETs. This bipolar transistor effect is activated in switch off-state and resulted in a greater OFF current. The parasitic bipolar junction transistor (BJT) activity is significantly affected by the drain region doping. Parasitic BJT effect is dependent on the doping of extension regions of source and drain of junctionless accumulation mode FET (JAMFET) and Nanowire MOSFETs.

Dipankar Ghosh et al. [13] in 2012 said that junctionless FETs can be used in low power devices provided: 1) greater channel length (in the region operating less than threshold voltage) inhibits short-channel effects; 2) underlap structure and the center

channel reduce the capacitances; 3) the simple fabrication process eliminates the need for source/drain; and 4) gain and early voltage can be improved by reducing electric field at the gate nearer to the drain.

Uygar Avci et al. [14] in 2015 modelled that Tunnel FET will be one of the future devices due to its steep slope less than 60 mv/decade, hence achieving less threshold and operating voltage.

Kathy Boucart and Adrian Mihai Ionescu [15] in 2007 demonstrated that, high-K material can improve the scaling of the Tunnel FET with double gate (DG TFET) and at the same time control of junction is also improved.

Eng-Huat Toh et al. [16] in 2007 proved that based on band-to-band tunnelling, the DG TFET's on-state drain current $I_{ON}$ is greatly influenced by the silicon film thickness $T_{Si}$. Band-to-band tunnelling must be modulated by a strong gate coupling at the source's location in centre of silicon film. The driving current and silicon volume accessible for band-to-band tunneling would both grow if the silicon film were to be thicker up to a certain degree. Over this threshold, the gate to channel coupling is lessened, which causes the on-state current to decrease.

New device architectures using both vertical monolithic and heterogeneous integration will provide growing functionality at historical rates for atleast 10 years, but expect further innovation after that [17].

Kartik Ganapathi, and Sayeef Salahuddin [18] in 2011 said that in homogenous Vertical Tunnel FET (VTFET), on current is low due to staggered bands. Inclusion of N+ pocket increases vertical tunneling hence on current is improved. Greater steepness in a hetero-VTFET's turn-on is caused by two factors: 1) the beginning of both tunneling in the pocket region and lateral tunneling beneath the pocket 2) the contribution of current's vertical tunneling component.

Sandeep Kumar et al. [19] in 2021 simulated that raising the work function value reduces leakage by improving gate controllability over the double gate JLT's channel region.

Girish Wadhwa and Jeetendra Singh [20] in 2020 demonstrated that small bandgap narrow band-bending brought on by the $Si_x Ge_y$ N+ pocket generates increased tunneling and steeper SS in TFET.

## 3. OBJECTIVES OF THE RESEARCH

The intention of the research work is to:

1. To simulate double gate recessed junctionless device using high k $HfO_2$ as a dielectric. Gate engineering to be done to reduce leakage. The characteristics that need to be looked into for the device are the threshold voltage ($V_{th}$), subthreshold swing (SS), OFF-current, ON-current, ON/OFF ratio.
2. To use low-k and high- and materials in recessed junctionless field effect transistor in order to improve its performance.
3. To design a VTFET device with binary gate electrode that has a gradually graded work function and air pocket. Investigations should be done on transconductance (gm), and transconductance generation efficiency ($T_{GE}$), ON-current ($I_{ON}$), subthreshold swing (SS).
4. To design a Vertical Tunnel FET structure with live molybdenum metal strip & low dielectric constant material in drain. The device is to be examined by the parameters $I_{OFF}$, subthreshold swing, threshold voltage, and $I_{ON}/I_{OFF}$ ratio.

## 4. RESEARCH PROBLEM

Nanoscale devices operate in the subthreshold region, which is characterized by a gate - source voltage less than threshold voltage, making subthreshold leakage an undesirable component of these devices. It not only affects the performance of the system but also impacts the margins available for design since leakage is related to process variation. In nanometer technology leakage is exponentially related to oxide thickness, temperature, supply voltage & channel length. Thin $SiO_2$ used as dielectric increases gate oxide leakage. Alternate materials like $HfO_2$ can be used to lessen leakage.

One of the alternative devices for conventional MOSFET is Junctionless FET. Modification of gate structure of the device, usage of high k material can be done to overcome gate leakage.

Threshold voltage and subthreshold current depends on channel length. Devices suffer from short channel effects as the channel length has reached the scaling limits. Hence structures with sufficient channel length can be designed supporting scaling effect.

## 5. PROPOSED METHOD

High k materials help to create structures for junctionless and tunnel FETs with less leakage. To lower $C_{GD}$ / Miller capacitance, vertical TFET architectures with $SiO_2$ at the drain are to be employed. The TCAD software is used to simulate the designed structures. An analysis is conducted on the effects of using materials with both high and low K counts.

### 5.1 Design of Modified Junctionless Multigate transistor with thin channel:

Recessed modified junctionless FET is designed with $HfO_2$ serving as the high-k dielectric medium. Gate engineering is done in this design. Modification of the oxide structure in gate can change the energy distribution of the carriers resulting in a decrease in off current. A recessed double-gate JLFET (R_DGJLFET) had a reduced subthreshold swing (SS), a lower $I_{OFF}$, and a significantly superior $I_{ON}/I_{OFF}$ when there were less carriers in the channel in the off state. Raising the work function value allows for enhanced gate control in the channel, which reduces $I_{OFF}$ and enhances $I_{ON}/I_{OFF}$. The rate at which the current decreases as soon as the transistor enters the off-state is measured by the parameter namely subthreshold swing (SS). SS of a typical FET is limited by the current production, which is dependent on thermionic emission, to 60 mV/decade. Low $I_{OFF}$ is suitable for little SS.

### 5.2 Enhancement in Recessed Modified Junctionless FET:

High k & low k dielectric constant materials are utilized in the device to modify the charge holding capacity at the source/channel junction and minimize the undesired capacitance at the drain/channel junction in addition to reducing the channel width in a junctionless transistor. The material having k=25 is used as the gate dielectric at the source-channel junction and $SiO_2$ is used at the drain-channel junction. This results in an enhancement of $C_{GS}$ -gate-source capacitance, a decrease in $C_{GD}$ -gate-drain capacitance, and minimization of charge concentration in the off state. Minimization of leakage at the drain region is an added merit of using low-k material. Gate-drain capacitance is decremented by dielectric material having k=3.9.

### 5.3 Design of a graded binary metal gate work function VTFET with air pocket:

The proposed structure is constructed with a binary alloy ($a_{\sigma}\ b_{1-\sigma}$) electrode, dielectric pocket and a linearly graded work function value. The work function of this linearly graded VTFET (LGWVTFET with air pocket) changes gradually with the combined metals σ (mole fraction) metric (A and B).

$$\phi(\sigma) = \sigma\phi_B + (1-\sigma)\phi_A$$

$\varphi_A$ and $\varphi_B$ - work functions of metal alloy.

Through linear variation and mole division, the work function is modified from 4.10 to 4.50. The work function value of the gate electrode ($a_{\sigma}\ b_{1-\sigma}$) is completely enforced and effected by 'a' at the source-channel interface, and is modulated in a linear manner, at the same time 'b' has a full effect at the channel-drain interface. The device structure also includes a dielectric pocket for improved tunnelling, increased ON current, and transconductance. The air pocket and binary metal work function combination increases the drive current and decreases SS. With lower SS and higher transconductance, the proposed structure sharpens the inclination of band twisting. An order for improvement in $I_{ON}$ is '1' and better transconductance is seen.

### 5.4 Reduced Subthreshold Swing in Vertical Tunnel FET using low work function live metal strip and low k material in the drain

In this paper, existing VTFET structure is taken for analysis [21] Thin channel and a large tunnel area enhances the device figure of merit [22]. To lessen undesired capacitance, the suggested design makes use of low-k dielectric in drain region. Cgd. A metal strip (Molybdenum) is placed at the source-channel interface. Impact of live metal strip and reduction of drain area is studied in terms of electron concentration, and tunneling rate. Live strip used has a compatible work function with $HfO_2$. The combination of metal strips & low k material at drain shows minimum $I_{OFF}$, good, reduced subthreshold swing, lower ambipolarity, and Miller capacitance- $C_{GD}$.

## 6. OVERVIEW OF THE RESULTS

The characteristics of junctionless field effect transistor structure with recessed channel is compared with the published model [19] in Figure1.

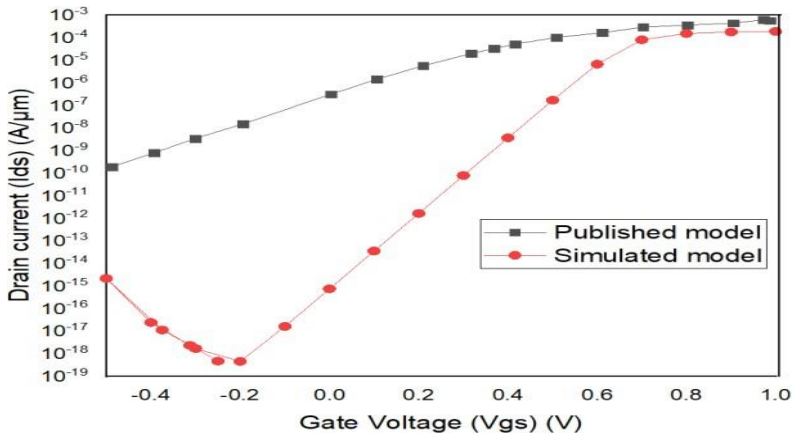


**Figure 1. Drain current of the published and simulated model [19].**

Figure 2. compares the transfer characteristics $I_{DS}$ vs. $V_{GS}$ for n-type JLFETs for different work function values from 4.6 to 5.0 eV. $1x10^{19}$ $cm^{-3}$ doping concentration is employed. Plotting of the graph is done for fixed $V_{DS}$ value 0.05 V and variable $V_{GS}$ = 0 to1.0 V.

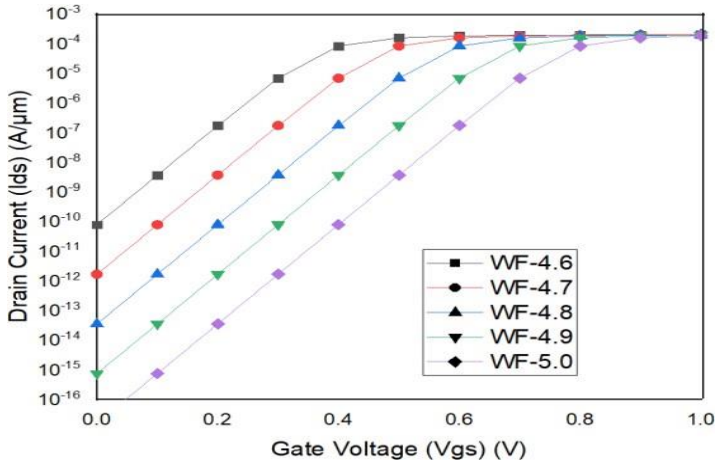


**Figure 2. Transfer properties between $I_{DS}$ and $V_{GS}$ for various gate work function values**

Figure 3 shows the current ratio vs. work function for an n-type JLFET at $V_{GS}$ = 0 to 1 V and $V_{DS}$ of 0.05 V.

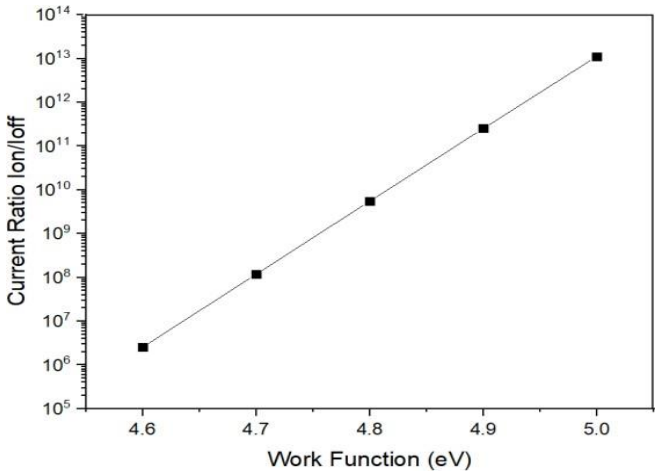


**Figure 3. $I_{ON}/I_{OFF}$ vs. Work function at $V_{DS}$ of 0.05 V and $V_{GS}$ = 0-1 V for an n-type JLFET.**

Because the leakage declines as the work function increases, it is noticed that the current ratio $I_{ON}/I_{OFF}$ rises.

Figure4. clearly illustrates the difference between the optimized junctionless field effect transistor and the published version [19].

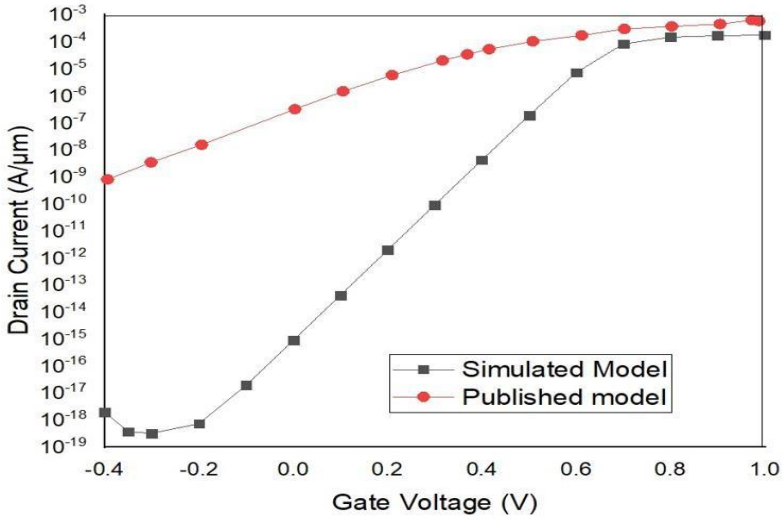


**Figure 4. Plot of Ids vs Vgs for the published model and optimized Recessed junctionless field-effect transistor [19].**

Figure 5. illustrates how the work function change affects threshold voltage.

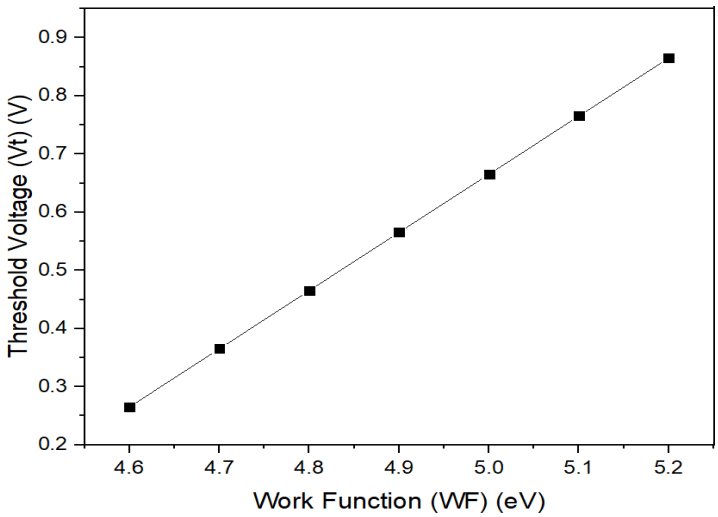


**Figure 5. Threshold voltage $V_{GS}$=0 to 1 V and $V_{DS}$=0.05 V for various work functions.**

The change in $I_{ON}/I_{OFF}$ for various work functions is shown in Figure 6. A small decrement in $I_{ON}$ value and more reduction in $I_{OFF}$ lead to enhancement of $I_{ON}/I_{OFF}$ ratio.

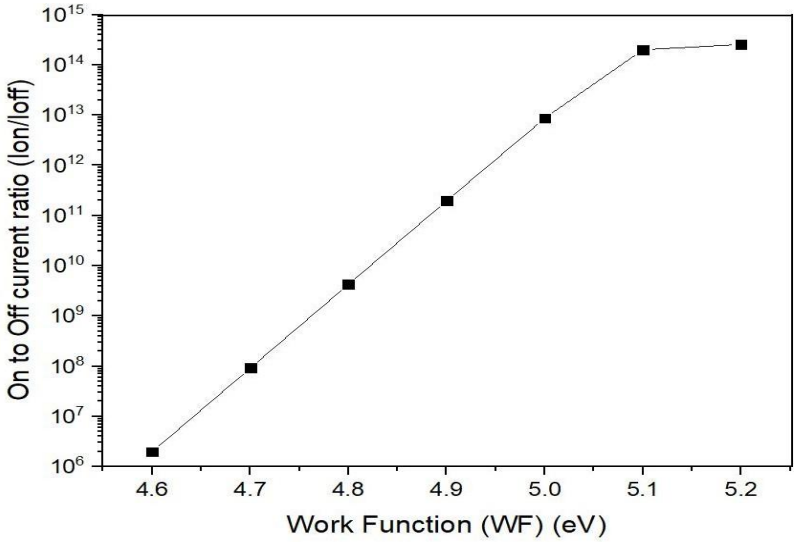


**Figure 6. $I_{ON}/I_{OFF}$ ratio in relation to Work function values at $V_{GS}$ = 0 to 1V and $V_{DS}$ = 0.05 V.**

Figure7. compares the published model [20] that uses the $Si_{0.55}Ge_{0.45}$ pocket with the designed VTFET with air pocket. The electric field is depicted in Figure 8. the presence of an air pocket causes an increase in electron concentration.

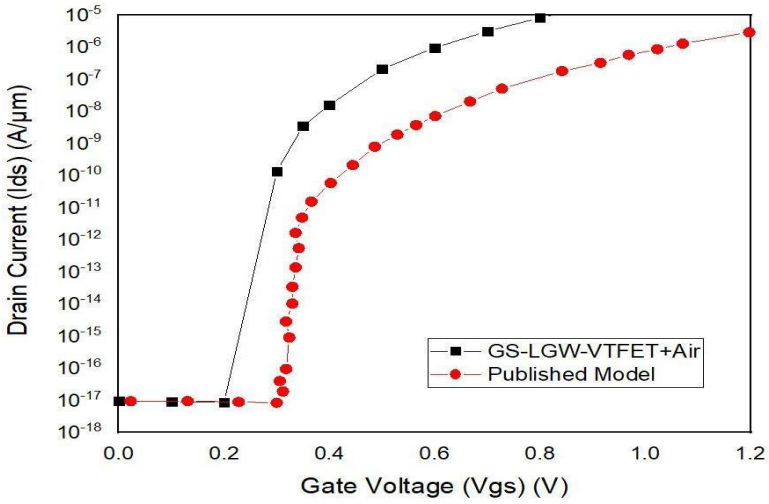


**Figure 7. $I_{DS}$ vs. $V_{GS}$ curve of the simulated device and published structure found in [20]**

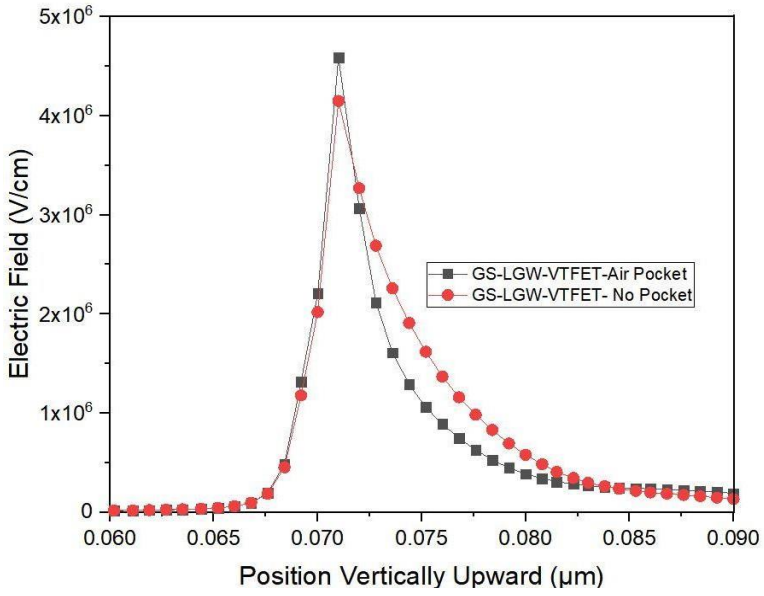


**Figure 8 – Electric field at $V_{DS}$ = 1 V.**

Figure 9. illustrates transconductance generation efficiency TGE = $gm/I_{DS}$ and greatest transconductance for the VTFET with air pocket, the topology with the minimum SS. Additionally, Figure.10 provides proof that the TGE is incredibly high at a lower bias of 0.2V for gate stacked linearly graded VTFETs (GS-LGW-VTFETs) with air pockets.

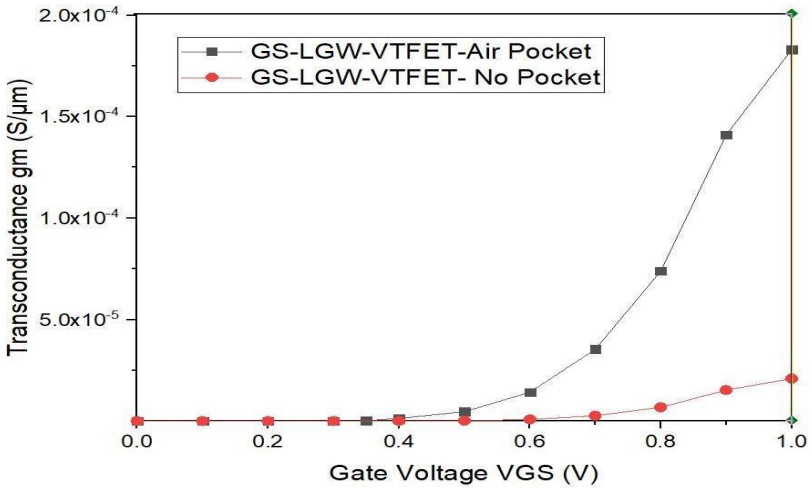


**Figure 9. Transconductance at $V_{DS}$ = 1 V.**

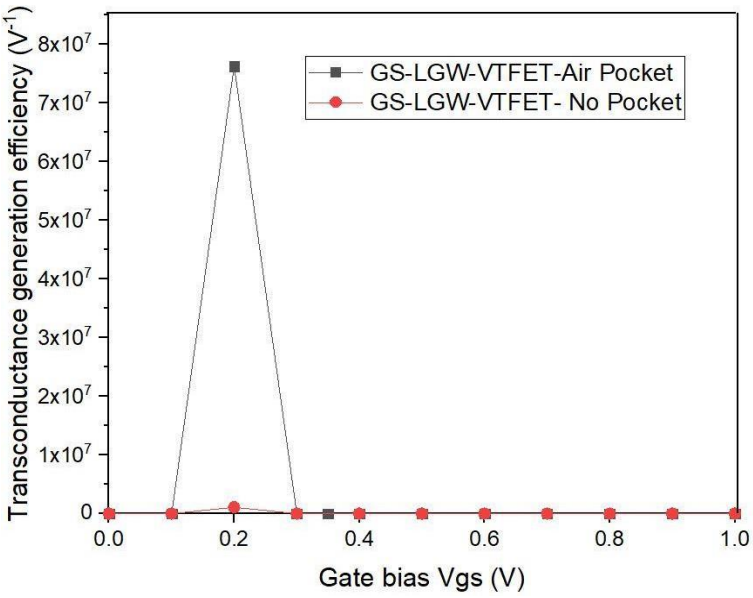


**Figure 10. Transconductance generation efficiency (TGE) at $V_{DS}$ value=1 V.**

Electron concentration of VTFET with low work function live strip and spacer, live strip and spacer alone is exhibited in Figure 11. Electron concentration is maximum for VTFET with live strip and spacer.

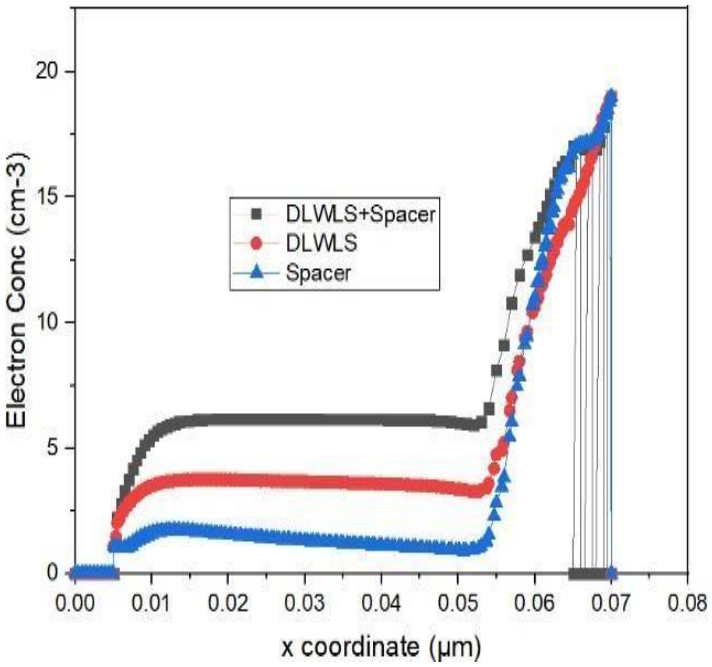


**Figure 11. Electron concentration in VTFET with DLWLS + Spacer, DLWLS & Spacer .**

As negative charge concentration increases electric field also increases. This is shown in Figure 12.

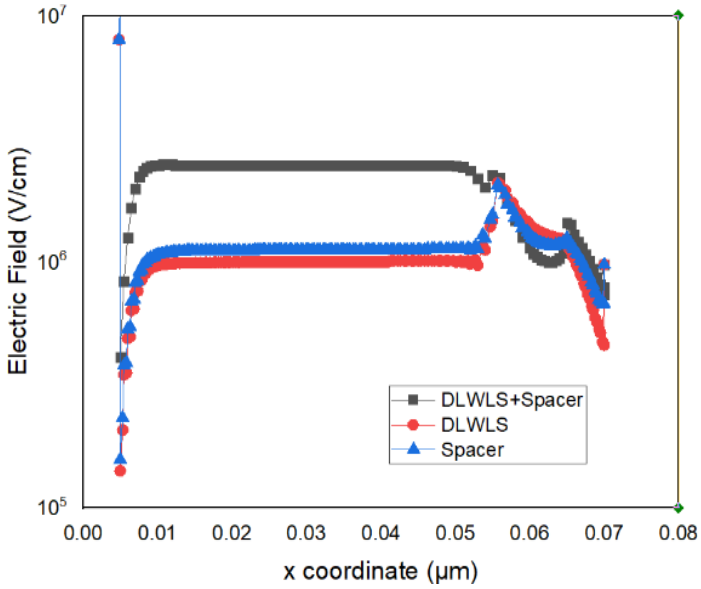


**Figure 12: Electric Field VTFET in DLWLS + Spacer, DLWLS & Spacer regarding Electric Field.**

The below Figure 13. shows the transfer characteristics of the 3 devices. Leakage current is minimum in the proposed model which is VTFET structure with Molybdenum and spacer.

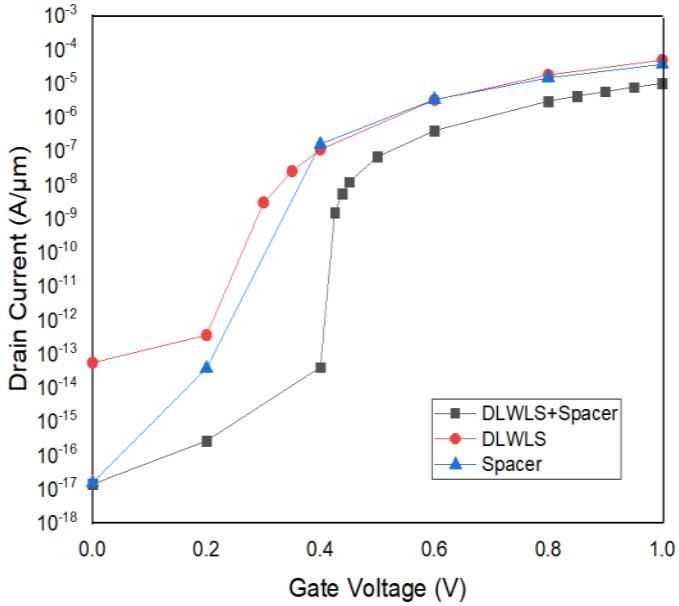


**Figure 13. Transfer characteristics of VTFET with DLWLS + Spacer, DLWLS & Spacer.**

Figures 14 shows the decrease in $C_{GD}$ respectively for the proposed model.

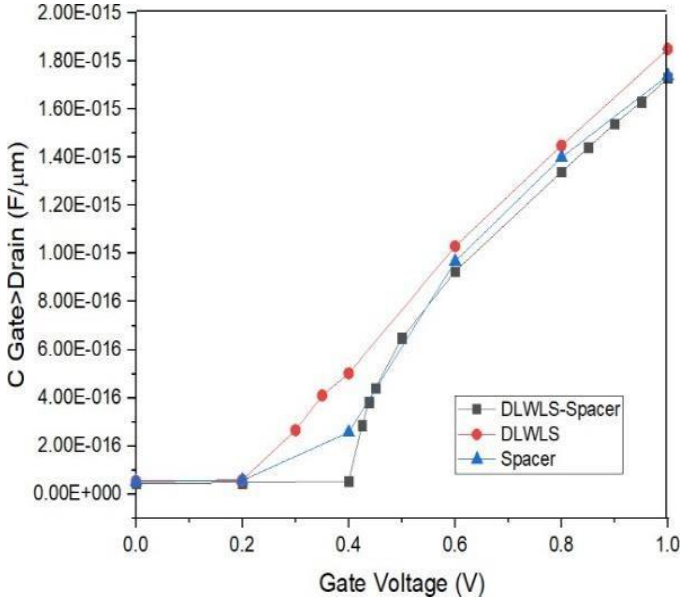


**Figure 14: Gate- drain Capacitance –voltage characteristics.**

## 7. ORGANIZATION OF THE THESIS

This dissertation is structured as eight chapters:

**Chapter 1**

**C**hapter1 details the drawbacks of $SiO_2$ dielectric in FET & its impact on the performance particularly leakage, scaling issues. Alternative to $SiO_2$ is high K materials their need & impact is discussed. An overview of leakage and its types is briefed. Engineering methods to reduce leakage has been listed. A short description of junctionless FET & Tunnel FET is given. Undesirable leakage has motivated to find techniques to reduce leakage. The advantages of $HfO_2$ have driven to lessen off current.

**Chapter 2**

Working principle of Junctionless FET &Tunnel FET is discussed. A review of the works that was done to understand leakage in Field effect transistor has been reported in this chapter. Impact of high k materials and drawbacks of $SiO_2$ is also reviewed. The chapter also provides insight into problems associated with conventional MOSFET and mechanism to lessen off current.

**Chapter 3**

A novel approach is given to lessen leakage in junctionless tunnel FETs. Recessed channel Junctionless Tunnel FET is built in the suggested construction utilizing $HfO_2$ as a dielectric material. To lower leakage current, the gate oxide thickness at the margins is increased relative to the channel oxide thickness at the center. The Atlas Silvaco TCAD simulator is used to replicate the intended structure and determine the behavior of several parameters, including drain current, $I_{ON}$, $I_{OFF}$, and subthreshold swing.

**Chapter 4**

This chapter details the improved recessed junctionless FET. To increase the charge at the source and decrease the undesirable charge at the drain junction, high & low dielectric constant materials are utilized at the source-channel junction and the channel-drain junction, respectively. The silicon channel of the recessed junctionless field-effect transistor is quite small. Channel width is decreased in order to decrease off current. In the off state, there is a reduction in the electron concentration in the channel region. Less

tunneling occurs within the device when the dielectric material is thicker around the borders than it is in the center.

**Chapter 5**

Using an air pocket with a graded binary metal alloy gate electrode - unique VTFET device is built. Instead of using multiple electrodes binary metal alloy is used whose work function is linearly varied, hence its molar fraction. Linearly graded electrode provides symmetric potential spread throughout channel. Presence of air pocket increases tunneling current. In terms of on current, subthreshold swing, and transconductance generation efficiency, their performance is compared with that of VTFETs in the absence of an air pocket.

**Chapter 6**

A Vertical Tunnel FET structure with live metal strip & low dielectric constant material is simulated and its performance metrics are analyzed. $SiO_2$ material is incorporated in the channel/drain region. Low work function live metal strip (Molybdenum) is placed in high k dielectric $HfO_2$ layer in source/channel region. We find the parameters threshold voltage, $I_{OFF}$, $I_{ON}/I_{OFF}$ ratio, subthreshold swing. The impact of live metal strip in the dielectric layer nearer to the source-channel is examined. Reduction of drain region is done by using dielectric layer which enhances the performance.

**Chapter 7**

This chapter summarizes the thesis and includes directions for future work that could be carried for development.

## 8. CONCLUSION

Various structures including Recessed Modified Junctionless Multigate Transistor, Optimized Recessed Modified Junctionless Multigate Transistor, Dual Material Gate Vertical Tunnel FET and VTFET with binary alloy gate, air Pocket have been proposed to increase transconductance while lowering subthreshold swing and incorporating high k $HfO_2$ to increase capacitance at the source/channel junction. Additionally, a Vertical TFET structure with Molybdenum live metal strips and high k and low k material are used to

obtain minimum subthreshold swing of 5mV/dec. Each proposed construction has its own special benefits and specifications. Therefore, all unique structures cannot be combined.

The junctionless FET device was gate-engineered by thickening the dielectric at the edges and narrowing the channel. Thin $SiO_2$ layer can leak through the gate oxide so $HfO_2$ is used as a dielectric material. High dielectric constant (20–25) of $HfO_2$ is 4-6 times greater than $SiO_2$. In this work threshold voltage ($V_T$), OFF-current, ON-to-OFF ratio, sub threshold swing (SS) of double-gate junctionless FETs have been analyzed for 4.6 to 5.0 eV work functions. The outputs indicate that the recommended structure is applicable for low power devices.

First, by altering the dielectric layer's structure, the leakage current is decreased. A junctionless field-effect transistor's recessed channel and dielectric materials—high & low k—are used in the construction of gate to increase charge holding capacity at the source-channel junction and reduce miller capacitance at the drain-channel junction. This study has calculated the threshold voltage, OFF-current, ON-current value, ON/OFF value of the recessed modified junctionless field-effect transistor for gate work function values varying from 4.6 eV to 5.2 eV. Consequently, low-power applications may benefit from the recommended JLFET.

The features of graded work-function binary metallic alloy $a_\sigma b_{1-\sigma}$ gate electrode with an air pocket in a vertically aligned TFET (V-TFET) are investigated. The suggested structure's performance metrics are evaluated and compared to industry norms. Metrics such device transconductance (gm), ON-current ($I_{ON}$), subthreshold swing (SS), and transconductance generation efficiency show that integrating LG-W with gate-stack V-TFET and air pocket, or SG-LG-VTFET with air pocket, improves working characteristics. A narrow band-bending is seen as a result of the LG-W and air pocket inclusion, leading to higher tunnelling and a steeper SS. A desirable occurrence to boost ON current is the dielectric pocket's increase in the electric field.

Better turn-off characteristics are achieved by designing a vertical TFET with $SiO_2$ in the drain, $HfO_2$ in the source and molybdenum live metal strips. Capacitance is enhanced by raising charge q by the use of a high k dielectric substance ($HfO_2$). An increase in i(t) flow within the device is the result of the increase in stored charge. $SiO_2$, a material with a low dielectric, is used at the drain-channel region. By doing this, charge stored in a parallel plate capacitor (gate-drain) and the drain region are decreased. It thus lowers undesired $C_{gd}$. An abrupt increase in electron concentration is caused by a metal strip put in the source-

channel interface, which speeds up tunneling. The suggested construction is contrasted with and without $SiO_2$ spacer at the drain and metal strips. The proposed structure achieved a better subthreshold swing of 5mV/dec.

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## LIST OF PUBLICATIONS

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